a data bus to which the CPU, the electrically programmable ROM and the memory are coupled; and

an address bus to which the CPU, the electrically programmable ROM and the memory are coupled,

wherein the electrically programmable ROM and the memory are allocated at mutually different address space of the CPU,

wherein the program includes an instruction changing a process of the CPU to a process for controlling a programming of the electrically programmable ROM based on the write control program stored in the memory, and

wherein the write control program has an instruction which returns the process of the CPU to a process based on the program stored in the electrically programmable ROM after completion of the process that controls the writing of the electrically programmable ROM.

~~23~~. (Amended) A microcomputer according to claim 21, wherein the ~~memory~~ which stores a write control program is a RAM that receives the write control program from the ROM.

~~24~~. (Amended) A microcomputer comprising:

an electrically programmable read only memory (ROM) including:

a first area to store a first program therein and

a second area to store data therein;

a memory storing a second program for controlling a writing to the electrically programmable ROM;

a central processing unit executing the first program and the second program,

a data bus to which the central processing unit, the electrically programmable ROM and the memory are coupled; and

an address bus to which the central processing unit, the electrically programmable ROM and the memory are coupled,

wherein the ROM and the memory are allocated in mutually different addresses in an address space of the central processing unit,

wherein the first program includes an instruction to change a process of the CPU to a process controlling a programming of the ROM based on the second program stored in the memory, and

wherein the second program includes an instruction to return the CPU to the process based on the first program in the ROM after completion of the process that controls the writing of the ROM.

28. (Amended) A method of writing data into an electrically erasable programmable ROM (EEPROM) under control of a CPU , wherein the EEPROM and the CPU are in a semiconductor substrate, the method comprising:

executing a first program in the EEPROM by the processing unit;

changing a process of the CPU executing the first program to a process executing a second program stored in a memoryformed in the semiconductor substrate, when an instruction in the first program is executed by the CPU;

executing the second program by the CPU in order to perform writing of data to the EEPROM by the CPU executing the second program; and

changing the process of the CPU executing the second program to the process executing the first program when an instruction in the second program is executed by the CPU,

wherein the memory and the EEPROM are disposed in mutually different addresses in one address space of the CPU.

29. (Amended) A method of writing data into an electrically erasable programmable ROM (EEPROM) according to claim 28, wherein the CPU executes a jump instruction as said instruction in the first program, and

wherein the changing of the process of the processing unit is changed when the CPU executes a return instruction as said instruction in the second program.

30. (Amended) A method of writing data into an electrically programmable ROM under control of a central processing unit , wherein the electrically programmable ROM and the CPU are in a semiconductor substrate, the method comprising:

executing a first program in the electrically programmable ROM by the central processing unit;